

PRE-REGULATOR WITH REVERSE CURRENT BLOCKING

Background of the Invention

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1. Field of the Invention

This invention relates generally to voltage regulators, and more particularly to a methodology that employs reverse current blocking via a lateral double-diffused MOS (LDMOS) device to block the current flow when the supply connection is reversed.

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2. Description of the Prior Art

Junction isolated IC processes must be protected against reverse supply connection. In many instances, this is done within the system, where an external component is placed to perform this function. In small, highly integrated systems
15 however, it is desired or required to eliminate the external blocking component. Known solutions consist of PMOS or bipolar PNP transistor protection. Such solutions, in certain applications such as pre-regulators, are not area efficient.

In view of the foregoing, it would be both beneficial and advantageous to provide
20 a reverse current blocking technique and that does not employ PMOS, bipolar PNP, or external circuit current blocking devices to block the current flow when the supply connection is reversed.

Summary of the Invention

To meet the above and other objectives, the present invention provides an N-channel MOS transistor that blocks the current flow when the supply connection is reversed. When connected properly, the body diode conducts to provide a start-up function. A pre-regulator using the N-channel MOS transistor also employs a bias generator to enable the low drop-out voltage function, allowing the output voltage to be very close to supply.

The pre-regulator is advantageous in that it eliminates the need to employ external blocking diodes or mosfets. Another advantage provided by the pre-regulator is that it allows for lower drop-out voltage performance than that achievable using an external diode. Yet another advantage provided by the pre-regulator is associated with lower system costs, offering a competitive advantage to end users; and a competitive advantage in low-cost competitive markets.

According to one embodiment, an apparatus comprises a reverse current blocking circuit devoid of PMOS, bipolar PNP, and external circuit protection devices, wherein the reverse current blocking circuit is operational to protect the apparatus against reverse current flow in a high side connected to a supply voltage and against reverse current flow in a low-side connected to ground.

According to another embodiment, an apparatus comprises means for protecting the apparatus against reverse supply voltage connections, wherein the reverse supply voltage connection protecting means is devoid of PMOS devices, bipolar PNP devices, and protection devices external to the apparatus.

According to yet another embodiment, an apparatus operates to pass a supply voltage to an output node below a desired regulation level, wherein the apparatus is protected against a reverse supply connection without use of PMOS, bipolar PNP, or external pre-regulator protection devices.

According to still another embodiment, a method of protecting an apparatus against reverse supply connections comprises the steps of:

providing an apparatus reverse current blocking circuit in electrical communication with an output node and that is devoid of PMOS devices, bipolar PNP
5 devices, and external circuit protection devices; and

preventing reverse current flow in at least one electrical path selected from the group consisting of a high side path connected to a supply voltage, and a low-side path connected to ground.

Brief Description of the Drawings

Other aspects and features of the present invention and many of the attendant advantages of the present invention will be readily appreciated, as the invention becomes
5 better understood by reference to the following detailed description when considered in connection with the accompanying drawing figure thereof and wherein:

The Figure is a schematic diagram illustrating a pre-regulator with reverse blocking capability according to one embodiment of the present invention.

10 While the above-identified drawing figure sets forth a particular embodiment, other embodiments of the present invention are also contemplated, as noted in the discussion. In all cases, this disclosure presents illustrated embodiments of the present invention by way of representation and not limitation. Numerous other modifications and
15 embodiments can be devised by those skilled in the art which fall within the scope and spirit of the principles of this invention.

Detailed Description of the Preferred Embodiments

The Figure is a schematic diagram illustrating a pre-regulator circuit 10 with reverse blocking capability according to one embodiment of the present invention. As stated herein before, junction isolated IC processes must be protected against reverse supply connection. In many instances, this is done within the system, where an external component is placed to perform this function. In small, highly integrated systems such as pre-regulator circuit 10 however, it is desired or required to eliminate the external blocking component. Known solutions, as also stated herein before, consist of PMOS or bipolar PNP transistor protection that are not efficient in certain applications such as pre-regulators.

Looking again at the Figure, the pre-regulator circuit 10 can be seen to include an LDMOS transistor 34. The LDMOS transistor 34 is configured to block the flow of supply current whenever the supply VDD connection is inadvertently reversed. When VDD is connected properly, the LDMOS 34 body diode conducts to provide a start-up function. A diode D2 (30) also serves to start up the regulator. A charge pump (bias generator) 14 is used to enable the low drop-out voltage function, allowing the output voltage VDDREG 16 to be very close to the supply voltage VDD. Since the LDMOS transistor 34 provides a lower specific on resistance than that achievable when using PMOS or bipolar PNP protection devices, it provides a solution with a very competitive size and cost.

A more detailed functional description of the pre-regulator circuit 10 is now described herein below with continued reference to the Figure. The input voltage appears at the VDD pin 18 at the top of the Figure. Under normal circumstances, this pin 18 is always positive with respect to the DVSS and SUB pins 20, 22 respectively, that eventually tie to the same point at ground (OV) potential. The function of the pre-regulator circuit 10 is to take the supply voltage at the VDD pin 18 and pass it through to VDDREG 16 below the regulation point (6V in one application) in a “Low-Drop-Out” manner (a low impedance is seen between the VDD and VDDREG pins 18 and 16

respectively; so the $I \cdot R$ drop seen these two pins 16, 18 is small). Above the regulation point (when $VDD - I \cdot R > V_{reg}$, where V_{reg} is 6V in one application), the “Regulator” block 24 pulls down the gate of MN0 (26) to hold the output at the regulation point. The function of the “Charge Pump” (bias generator) block 14 is to form a bias current for the
5 output of the regulator 24 to work against and to also ensure that there is potentially enough excess voltage on the gate of MN0 (26) to ensure that it is in a low on-resistance area of operation.

Resistor R5 (28) and diode D2 (30) are provided for start-up, when the charge
10 pump 14 has not been functioning, and the gate of MN0 (26) is very close to ground. In this instance, MN8 (32) is off, and current flows into the node connected to the gate of MN0 (26), pulling it up, and in turn allowing VDDREG 16 to rise. Once there is voltage at the output, the charge pump 14 will begin to operate and assist in getting voltage to MN0 (26). When regulation is attained, MN8 (32) is turned on, which reverses the diode
15 D2 (30), disabling the start-up. It should be noted that MN8 (32) is not essential to the operation of the circuit 10 as a whole, but is present only to reduce the dependence of VDDREG 16 on VDD.

In normal operation, HV ISO (12) is not important when input voltages much in
20 excess of the regulation point are present. In this case, MN1 (34) presents itself as a diode (the inherent junction between the source and drain of MN1 (34) – it is physically impossible to remove this part of the device). In the case of low-dropout operation, MN1 (34) is turned on via the bias generator (charge pump) 14, charging the gate of MN1 (34) through D1 and R3. In this mode of operation, MN1 (34) is turned on, allowing it to
25 shunt the diode, thereby reducing the dropout voltage. It should be noted that the forward biasing of this device (MN1 (34)) junction creates a parasitic PNP device with its collector at substrate; so it may be advantageous to actually turn this device on in some cases. A second charge pump (not shown) can be employed to do this, by injecting charge into the gate of MN1 (34).

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Resistor R20 (36) forms a low-pass filter with capacitor C2 (38) to filter out the noise caused by the operation of the charge pump. The MET1 resistor R0 (40) is not essential to the operation of the circuit 10, but is used in this embodiment as a current measurement device by which MN0 (26) can be turned-off in the case of an overload condition at the output, VDDREG 16. This feature is not shown.

In reverse connection, the VDD pin 18 will go below ground, and current flow must be controlled. If MN0 (26) were simply to have its drain connected to VDD 18, the circuit 10 would be much simpler; but the presence of the deep NWELL drain on this device (MN0 (26)) means that it has a forward-biased junction present between substrate, SUB 22, (ground) and VDD 18 in the instant case. In order to prevent this undesirable condition, the present inventors connected two devices (MN0 (26) and MN1 (34)) with the drains (NWELL regions) common. In this way, current can be controlled in the case of either polarity: MN0 (26) controls in normal operation, and MN1 (34) controls flow (prevents it) in reverse conditions.

MN1 (34) prevents reverse current flow in the following manner: The isolated HV_ISO transistor 12 is biased on by diode D5, which holds the gate of MN1 (34) to VDD. In this way, the gate-source voltage, V_{gs} , of MN1 (34) is zero and this device is then biased off. Reverse flow will also occur from MN8 (32) and diode D5 (42); but this is controlled by the resistors 28, 44 respectively placed in series with them between VDD 18 and ground.

In view of the above, it can be seen the present invention presents a significant advancement in the art of voltage regulator technology. Further, this invention has been described in considerable detail in order to provide those skilled in the reverse current blocking art with the information needed to apply the novel principles and to construct and use such specialized components as are required. In view of the foregoing descriptions, it should further be apparent that the present invention represents a significant departure from the prior art in construction and operation.

However, while particular embodiments of the present invention have been described herein in detail, it is to be understood that various alterations, modifications and substitutions can be made therein without departing in any way from the spirit and scope of the present invention, as defined in the claims which follow.